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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,036	10/05/2000	Richard A. Mann	09785980-0021	9051

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EXAMINER
KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/680,036	Applicant(s) MANN ET AL.	
	Examiner Donghee Kang	Art Unit 2811	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 50-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 50-56* is/are rejected.

7)☒ Claim(s) *57 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgment

1. Applicant's Amendment and Response to Paper No.5 have been entered and made of Record. New claims 50-58 have been added. Therefore, claims 1-18 & 50-58 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-9, 17-18 & 50-54** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yiannoulos (US 5,942,775) in view of Hsieh et al. (US 6,448,595).

Regarding claim **1**, Yiannoulos teaches a sensor having a transistor with a gate, comprising (Fig.6):

a well region (634) formed beneath the source (605') such that a portion of the well region extends partially beneath the gate (603'); a channel disposed between the well region and the drain beneath the gate, the channel having a predetermined length; and a detection device coupled to the drain (605) by a signal path, wherein the channel allows the detection device to be reset to a predetermined state.

Yiannoulos does not teach the gate located partially over a source and a drain regions. However, Hsieh et al. in Fig.2F teach the gate electrode (206a) located partially over a source and a drain regions (212 & 213). Therefore, it would have been obvious

to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Hsieh into the Yiannoulos's device, since if the gate does not extend to the source and drain diffusion regions, an incomplete channel will be formed and the device will not operate properly. To avoid this possibility, the standard gate electrode processing calls for some overlap of the gate past the source and drain edges.

Regarding claims **2 & 50**, Yiannoulos teaches a sensor having a transistor with a gate, comprising (Fig.6):

a well region (634) formed to contain one of the source (605') and drain (605) such that a portion of the well region extends partially beneath the gate; an implant (636) formed in the substrate to extend between the well region and the other of the source and the drain; and a detection device coupled to the drain (605) by a signal path, wherein the implant allows the detection device to be reset to a predetermined state.

Yiannoulos does not expressly teach the implant region increasing a surface threshold of the transistor. However, it is acknowledged in the art that a buried channel formed by implantation is the most valuable tool for controlling threshold voltage in transistor and the implant region (636) of Yiannoulos would increase the threshold voltage.

Yiannouls does not expressly teach the detection is reset when a voltage that is greater than or equal to the surface threshold of the transistor is present on the gate. Notes that as the voltage on the gate electrode increases, electrons are attracted to the surface in a channel region. At some voltage level, the electron density at the surface will exceed the hole density. At this voltage, the surface has inverted polarity from the p-

type of the original substrate to an n-type inversion layer directly under the gate electrode. The voltage at which the surface inversion layer forms is called the threshold voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a voltage that is greater than the surface threshold voltage to the gate electrode in order to make the transistor "on" state, hence resetting the detection.

Yiannoulos does not teach the gate located partially over a source region and a drain region. However, Hsieh et al. in Fig.2F teach the gate (206a) located partially over a source and a drain regions (212 & 213). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Hsieh into the Yiannoulos's device, since if the gate does not extend to the source and drain diffusion regions, an incomplete channel will be formed and the device will not operate properly. To avid this possibility, the standard gate electrode processing calls for some overlap of the gate past the source and drain edges.

Regarding claims **3 & 51**, Yiannoulos as modified by Hsieh does not expressly teach that the surface threshold voltage of transistor is increased to at least 0.8 volts. Since the threshold voltage determines the requirements for tuning the MOS transistor on or off, it is able to adjust threshold voltage in designing the device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the threshold voltage in order to obtain a desired transistor.

Regarding claim 4, Yiannoulos as modified by Hsieh teaches the implant is formed to extend between the well region and the drain.

Regarding claim **5**, Yiannoulos as modified by Hsieh teaches the implant having a dopant concentration that is less than the well region.

Regarding claim **6**, Yiannoulos as modified by Hsieh does not teach the implant is a shallow boron implant. It is conventional in the art to provide doped semiconductor layer to achieve desired electrical properties and to use boron when p-type implants are required. It would have been obvious to one of ordinary skill to select a conductivity type that is appropriate for the type of device being manufactured and using boron in the implant step, since it is a known material well suited for intended purpose.

Regarding claims **7, 9 & 53-54**, Yiannoulos as modified by Hsieh does not teach that the predetermined length of the material is at least 20 percent greater than a process minumum and the gate has a gate length approximately two times a process minimum. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the length of the channel and gate electrode, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim **8**, Yiannoulos as modified by Hsieh does not teach that the drain is formed by a phosphorous implant level of approximately $2e^{12}cm^{-3}$. It is conventional in the art to vary the implant energy to achieve the desired implant depth or concentration. It would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the implant dose in order to obtain a desired concentration and/or depth.

Regarding claim **17**, Yiannoulos as modified by Hsieh teaches the detection device is a photo-detector.

Regarding claim **18**, Yiannoulos as modified by Hsieh teaches the photo-detector is a photodiode.

Regarding claim **52**, Yiannoulos as modified by Hsieh teaches the gate has a predetermined length and the implant extends approximately a half of the predetermined length of the gate.

4. Claims **10-16 & 55-58** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yiannoulos in view of Hsieh et al. and further in view of Fratin et al. (US 5,977,591).

Regarding claims **10, 12-13 & 55**, Yiannoulos teaches a sensor, comprising (Fig.6):

a transistor having a source (605'), a drain (605) and a gate (603') located between the source and drain; a well region (634) formed to contain one of the source and the drain and to extend partially beneath the gate.; and a detection device coupled to the drain by a signal path, wherein the channel is a p-type.

Yiannoulos does not teach the gate located partially over a source and a drain regions. However, Hsieh et al. in Fig.2F teach the gate electrode (206a) located partially over a source and a drain region (212 & 213). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Hsieh into the Yiannoulos's device, since if the gate does not extend to the

source and drain diffusion regions, an incomplete channel will be formed and the device will not operate properly. To avoid this possibility, the standard gate electrode processing calls for some overlap of the gate past the source and drain edges.

Neither Yiannouls nor Hsieh teaches the gate is divided into a p-type region and an n-type region. However, Fratin et al. in Fig.1 teach the gate (8) including a p-type (14) and an n-type (13), wherein the p-type substrate is in proximity to the p-type region of the gate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the gate structure of Yiannouls with the gate structure as taught by Fratin in order to create shallow extensions to the active regions. Such modification would provide Yiannouls with tapering the electric field in border areas between the channel and the source/drain regions.

Regarding claims **11 & 56**, cited prior art does not teach the predetermined length of the gate is approximately two times a process minimum. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the length of the channel and gate electrode, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim **14**, cited prior art does not teach that the drain is formed by a phosphorous implant level of approximately $2e^{12}cm^{-3}$. It is conventional in the art to vary the implant energy to achieve the desired implant depth or concentration. It would have

been obvious to one of ordinary skill in the art at the time the invention was made to vary the implant dose in order to obtain a desired concentration and/or depth.

Regarding claims **15-16**, neither Yiannouls nor Hsieh teaches an implant region, which is formed by a boron implant located in the drain extending under the p-type region of the gate. However, Fratin in Fig.1 teaches the implant region (5) located drain extending under the p-type region of the gate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Fratin with Yiannouls as modified by Hsieh in order to achieve a high breakdown voltage.

Allowable Subject Matter

5. Claims **57-58** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1-18 and 50-58 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

dhk
March 6, 2003

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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